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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/085,889

02/28/2002

Michael J. Rendon

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05/19/2004

FREESCALE SEMICONDUCTOR, INC.  
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EXAMINER

DIAZ, JOSE R

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/085,889

Applicant(s)

RENDON ET AL.

Examiner

José R Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 4-10, 12-19, and 21-22 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. (US Pat. No. 5,565,697) in view of Talwar et al. (US Pat. No. 6,300,208 B1), cited by applicant.

Regarding claims 1-2, 13, 16, and 19, Asakawa et al. teaches a method of forming a semiconductor device comprising the steps of: placing an energy absorbing layer (5) above the substrate (2) (see figs. 5 and 7); forming a semiconductor layer (14) above the energy absorbing layer (see fig. 5 and 7); forming a control electrode (40)

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(see figs. 5 and 7); forming first and second current electrodes (34, 36) within the semiconductor layer (14) (see figs. 5 and 7).

However, Asakawa et al. is silent with respect to the limitation of annealing or exposing the substrate to an energy source to electrically activate the source/drain regions. Talwar et al. teaches that is well known in the art to activate the source/drain regions (5,6) by using a laser (10) (see fig. 2F and col. 7, lines 15-20) with a wavelength of 100-1200 nm (see col. 7, lines 18-21).

Asakawa et al. and Talwar et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to anneal or expose the substrate to an energy source (e.g. a laser with a wavelength of 100-1200 nm) for electrically activating the source/drain regions. The motivation for doing so, as is taught by Talwar et al., is to activate the source/drain regions (col. 4, lines 26-33 and col. 7, lines 13-15). Therefore, it would have been obvious to combine Talwar et al. with Asakawa et al. to obtain the invention of claims 1-2, 4-10, 12-19 and 21-22.

Regarding claims 4-5, Talwar et al. teaches that is well known in the art to control the energy source by setting the wavelength of the light source to about 800 nm or more (see col. 7, lines 18-21).

Regarding claim 6, Talwar et al. teaches that is well known in the art to expose the energy-absorbing layer to an energy source (10) by positioning the energy source (10) to be above the integrated transistor device the substrate (2) (see fig. 2F).

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Regarding claim 7, Asakawa et al. teaches that the absorbing material (5) is made of, for example, tungsten and titanium (see col. 2, line 37-40).

Regarding claim 8, Asakawa et al. teaches that the semiconductor layer (14) has at least one of Si, Ge or GaAs (see col. 2, lines 35-36).

Regarding claim 9, Asakawa et al. teaches providing an insulating layer (38) between the energy absorbing layer and the control electrode (see figs. 5 and 7).

Regarding claims 10 and 17, Asakawa et al. teaches implementing the substrate as an insulator (4) (see figs. 5 and 7).

Regarding claims 12, 14 and 18, Asakawa et al. teaches the limitation of forming isolation regions (26, 30) (see figs. 5 and 7).

Regarding claim 15, Talwar et al. teaches that it is well known in the art to process a portion of the control electrode to comprise silicon having a higher melting temperature than the first and second current electrodes (see col. 5, lines 40-45) and processing the first and second current electrodes to comprise amorphous silicon (see col. 7, lines 7-12).

Regarding claim 21, Asakawa et al. and Talwar et al., as stated above, teach the claimed method of forming a device in which the source and drain regions are activated by a laser annealing step. With regards to the claimed resistivity, it is well known in the art that the resistivity of the source and drain regions is improved by laser annealing such regions. Thus, it would have been obvious to one of ordinary skill in the art to lower the resistivity from 0.1 ohm-cm to 0.001 ohm-cm, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in

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the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The ordinary artisan would have been motivated to modify Asakawa et al. and Talwar et al. in the manner described above for at least the purpose of activating the source and drain region.

Regarding claim 22, Asakawa et al. further teaches an energy-absorbing layer of an electrically insulating material (4) (see figs. 5 and 7).

Claim 3, 11 and 20 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Asakawa et al. (US Pat. No. 5,565,697) in view of Talwar et al. (US Pat. No. 6,300,208 B1), and further in view of Chan et al. (US Pat. No. 6,057,212).

Regarding claim 3, a further difference between the prior art and the invention is the limitation of bonding the semiconductor layer to the energy-absorbing layer. However, Chan et al. teaches that it is well known in the art to form the semiconductor layer by bonding the semiconductor layer (3) to the energy-absorbing layer (5) (see Fig. 1).

Asakawa et al., Talwar et al. and Chan et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further include the limitation of bonding the semiconductor layer to the energy-absorbing layer. The motivation for doing so, as is taught by Chan et al., is to provide a conductive layer that does not interfere with semiconductor manufacturing processes (col. 2, lines 10-14). Therefore, it would have been obvious to further combine Chan et al. with Asakawa et al. and Talwar et al. to obtain the invention of claims 3, 11 and 20.

Regarding claims 11 and 20, Chan et al. further teaches providing an adhesion layer (325) between the energy-absorbing layer (4, 320) and the semiconductor layer (3, 335) (see Figs. 1 and 3).

### ***Response to Arguments***

Applicant's arguments filed March 11, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In the instance case, the examiner relies on Talwar et al. to show that using a light source to activate the source and drain regions is within the level of ordinary skill in the art (col. 1, lines 31-33 and 43-46). Thus, it is obvious to one of ordinary skill in the art to use a laser to activate the source and drain regions (34, 36) of Asakawa et al., and therefore, it is inherent to attribute the function of absorbing and transferring energy to the tungsten layer (5) of Asakawa et al.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

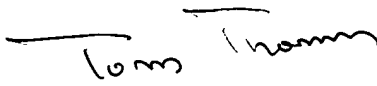
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD  
5/16/04

  
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